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(54) GENERALIZED LOGIC DEVICE

(71) We, HONEYWELL INFORMATION SYSTEMS LIMITED, a British Company, of Honeywell House, Great West Road, Brentford, Middlesex, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to devices which can be preset to perform any one of a wide variety of logic functions.

With the development of integrated circuits, and more particularly of LSI (Large Scale Integration) techniques, the number of circuit components or individual logic elements accommodated in a single device is becoming very large. The cost of such LSI devices is heavily dependent on the quantity to be made, since the cost of the initial design and start-up is high while the subsequent cost per device is low.

Whereas in many cases the quantity of devices required will be sufficient to render the initial costs insignificant, in the case of complex computer equipment the quantities of a device performing any particular function will usually be too small to justify its production in LSI form. In other words, a very large number of devices of different functions will be required, each one in only a small quantity.

The object of the present invention is to provide a logic device suitable for production in LSI form and capable of being preset to perform any one of a wide variety of logic functions. Such devices can be made in large quantities, and used in different ways to perform a wide variety of particular functions required in different circumstances.

Accordingly the invention provides a generalised logic device comprising a set of logic elements whose inputs and outputs form rows and columns respectively of a rectangular matrix of lines; gates interconnecting the row and column lines at their intersections; a corresponding matrix of storage devices controlling these gates; and means for setting the storage devices to a desired combination of states.

The storage devices thus define the particular interconnections of the inputs and outputs of the logic elements, and thus the overall function which they perform. The input and output lines of the device are preferably included in the matrix in the same way as the output and input lines, respectively, of the logic elements.

An example of the invention will be described more fully with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a generalised logic device, and

Figure 2 is a partial block diagram of the matrices of lines and storage devices.

Referring first to Figure 1, block 10 is a set of suitably chosen logic elements, such as gates of one or more types, flip-flops, etc. These are coupled to a matrix 11, the outputs 12A from the elements 10 and the inputs 12B to the device as a whole forming its columns and the inputs 13A to the elements 10 and the outputs 13B of the device as a whole forming its rows. At each intersection of a row and column in the matrix 11, an AND gate connects the column line to the row line. Associated with the matrix 11 is a matrix 14 of flip-flops, each AND gate in the matrix 11 being controlled by a corresponding flip-flop in the matrix 14. By setting the flip-flops of matrix 14 to appropriate states, any desired pattern of interconnections between the logic elements 10 can be set up, each row line of matrix 11 acting as a distributed OR gate combining signals applied thereto from the column lines via those AND gates of matrix 11 which are enabled.

The flip-flop matrix 14 is fed from an address register 15 and a data register 16, fed in turn over line 17 and lines 18 respectively from an interfacing unit 19 controlled via lines 20. When the device is in use as, e.g. a peripheral to a central processing unit of a computer, the inputs 12B and outputs 13B will be connected with other logic devices, etc., while the inputs 20 will be connected to a data highway, and the computer memory will permanently contain information for setting up the logic device. Each

time the computer is switched on, a preliminary period will be devoted to setting up this logic device (and other similar devices). The setting up information will be fed over the data highway and lines 20 to the interfacing unit 19, which will convert it to the appropriate form. In the arrangement illustrated, the address register 15 is arranged to count up so as to address each row of matrix 14 in turn, and the data register 16 is fed with the appropriate setting bits for each row in synchronism with the address register 15.

Figure 2 shows a small section of matrices 11 and 14 and logic elements 10 in more detail. Two column lines 12—1 and 12—2 and two row lines 13—1 and 13—2 of the matrix 11 are shown, lines 13—1 and 13—2 feeding a logic element 10—1 (a NAND gate) which feeds line 12—2. Each column line is connected to each row line by an AND gate; gate 11—1 is one such gate, connecting column line 12—1 to row line 13—2. Associated with each such AND gate is a flip-flop of matrix 14; flip-flop 14—1 is the flip-flop associated with AND gate 11—1. The state of this flip-flop determines whether the associated AND gate 11—1 is enabled or disabled, i.e. whether or not signals on line 12—1 are coupled onto line 13—2.

The matrix 14 includes, in addition to the flip-flops 14—1, etc., row lines 15—1, 15—2, etc. from the address register 15 and column lines 16—1, 16—2, etc. from the data register 16. Each flip-flop is associated with one row and one column line, flip-flop 14—1 being associated with row line 15—1 and column line 16—2. Energization of a row line causes each flip-flop fed from it to be set to the state of the signal applied simultaneously to the column line feeding it. Thus the flip-flops may be set to any desired combination of states.

Of course, many variations in detail may be made to the manner in which the flip-flops of matrix 14 are set up. For example, most of the flip-flops will be required to feed logical "0"s to the gates of matrix 11, only a few "1"s being required. The information fed in over lines 20 may therefore be in a different form from that fed to the register 16, and the advance of the address register may be in variable steps.

The matrices 1 and 14 may conveniently be arranged substantially as indicated in Figure 2. The logic elements 10 may be arranged physically within the matrix, for example along one diagonal; or the matrices may be "folded" along a diagonal to form two physically triangular and superimposed matrices, with the logic elements arranged adjacent to the hypotenuse of the triangle.

It should be apparent that for a given set of logic elements (gates, flip-flops, etc.) 10, the deviec can be set to perform every possible logical function which can be performed by interconnecting them; and, of course, the logical functions which can be performed by any subset of them. In other words, the device is a completely general logic device within the limits set by the number and type of logic elements 10. The bit pattern required for setting up the flip-flop matrix 14 may be determined by the designer by pencil and paper, or computer programs may be developed which will calculate suitable patterns from a definition of the overall function required.

WHAT WE CLAIM IS:—

1. A generalised logic device comprising a set of logic elements whose inputs and outputs form rows and columns respectively of a rectangular matrix of lines; gates interconnecting the row and column lines at their intersections; a corresponding matrix of storage devices controlling these gates; and means for setting the storage devices to a desired combination of states.

2. A generalized logic device according to claim 1 wherein the input and output lines of the device are included in the matrix of lines as columns and rows respectively therein.

3. A generalized logic device substantially as herein described with reference to Figure 1 of the accompanying drawings.

4. A generalized logic device substantially as herein described with reference to Figures 1 and 2 of the accompanying drawings.

For the Applicants,
J. D. LOVERIDGE.

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1444084 COMPLETE SPECIFICATION
1 SHEET This drawing is a reproduction of the Original on a reduced scale.

Fig. 1.

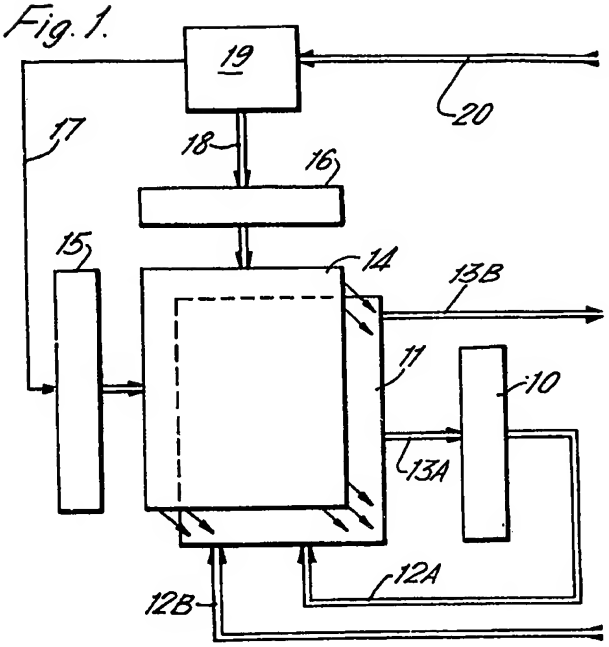

Fig. 2.